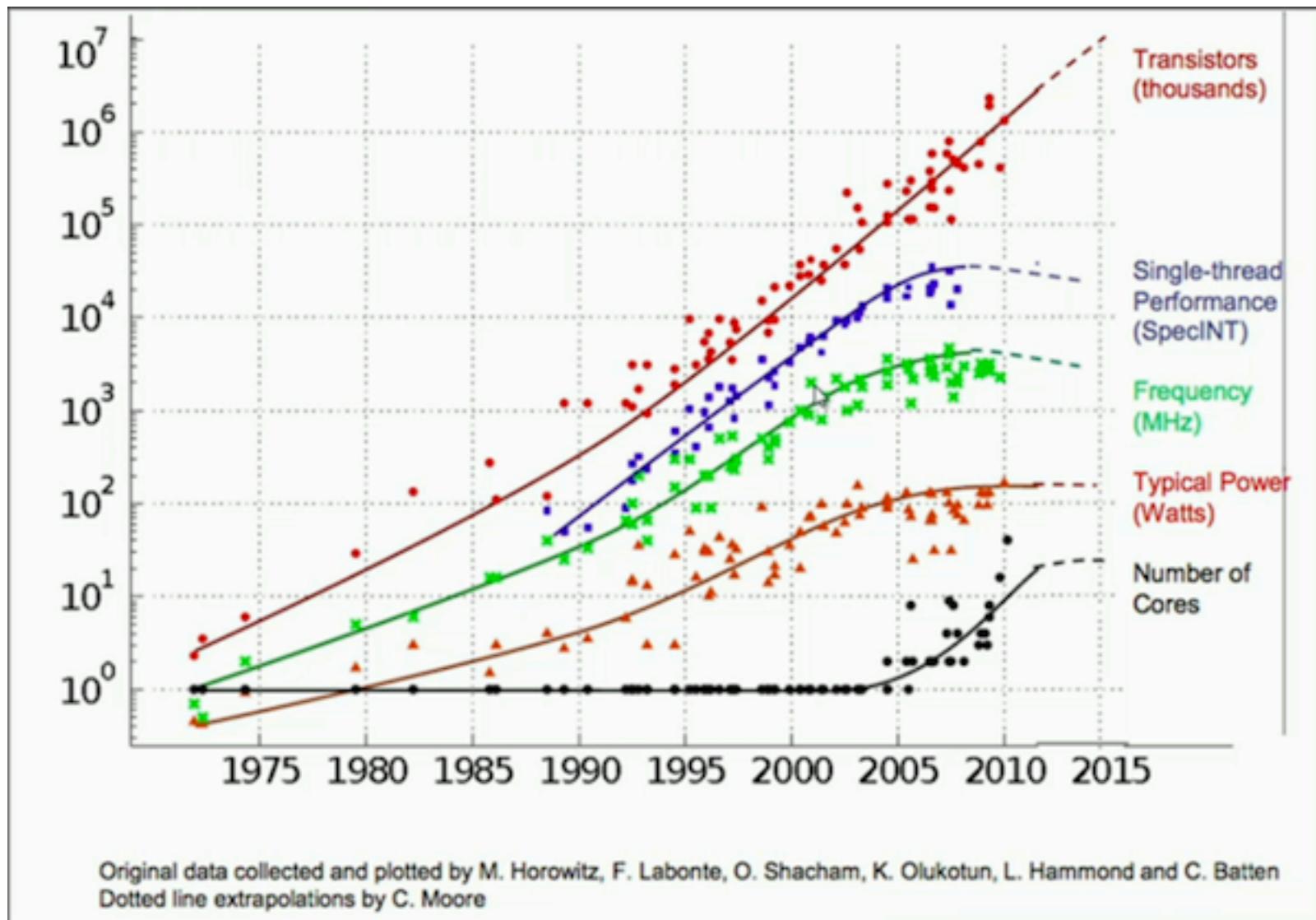


Architetture parallele

Legge di Moore



Parallelismo in CPU single-core

Operazioni
scalari

$$\begin{array}{ccc} A_0 & + & B_0 = C_0 \\ A_1 & + & B_1 = C_1 \\ A_2 & + & B_2 = C_2 \\ A_3 & + & B_3 = C_3 \end{array}$$

addl %eax, %ebx
addl %ecx, %edx
...

paddd %xmm0, %xmm1

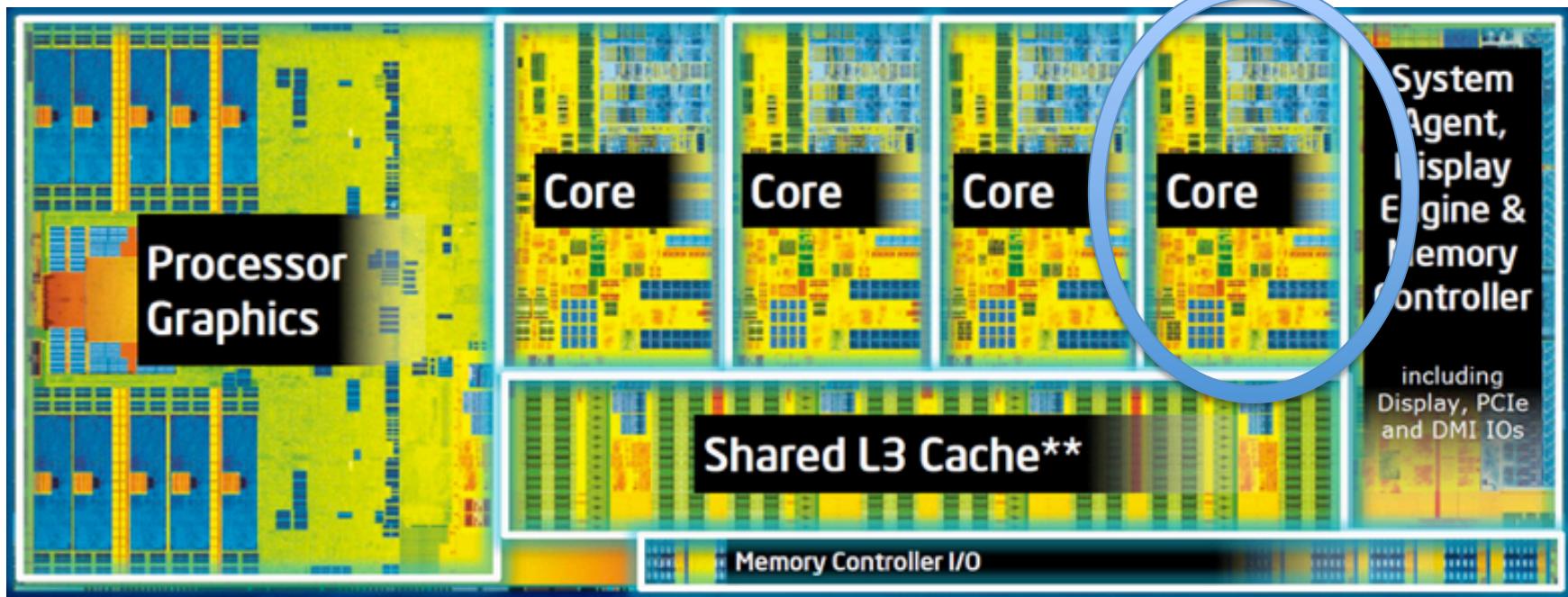
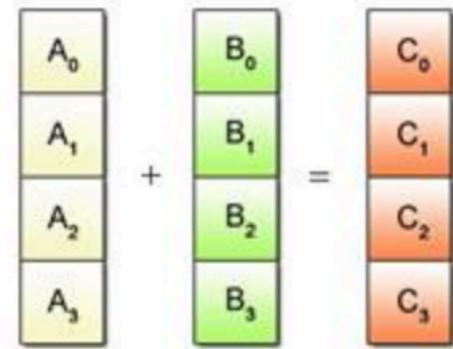
$$\begin{array}{ccc} A_0 & + & B_0 = C_0 \\ A_1 & & B_1 = C_1 \\ A_2 & & B_2 = C_2 \\ A_3 & & B_3 = C_3 \end{array}$$

Operazioni
vettorizzate
(SSE)



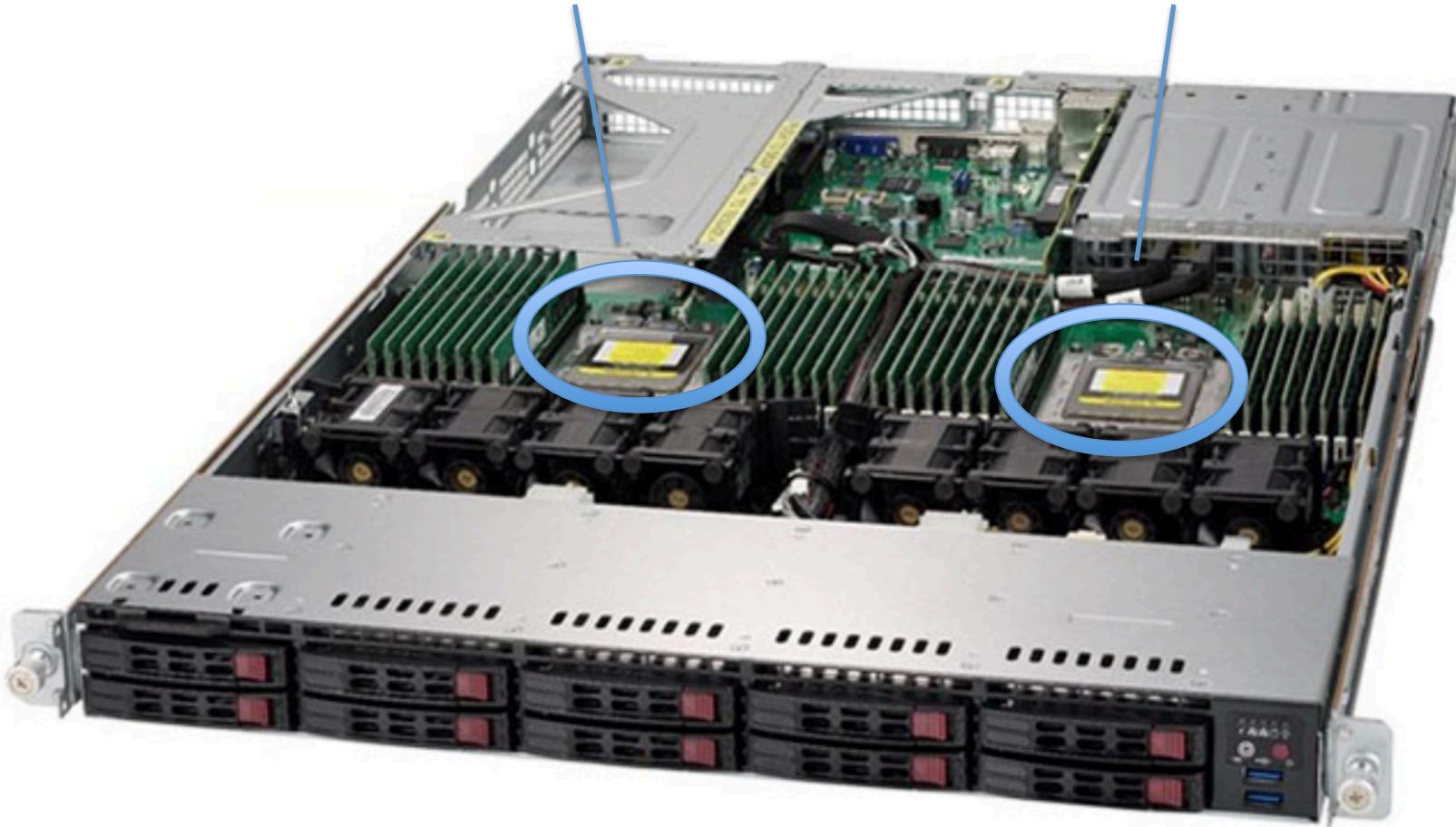
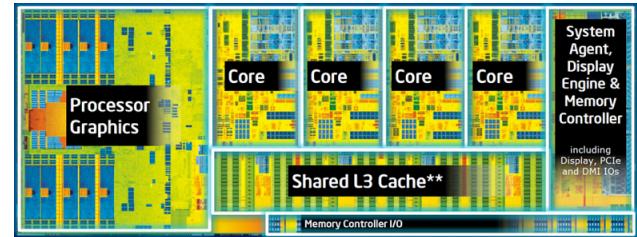
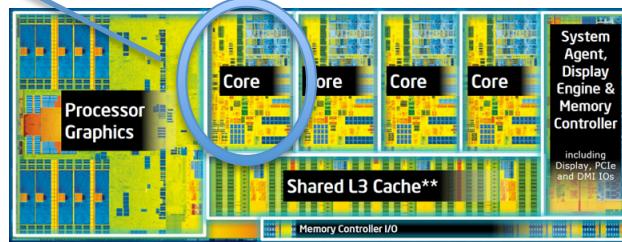
Intel
Pentium 4
2000-2008

CPU multi-core

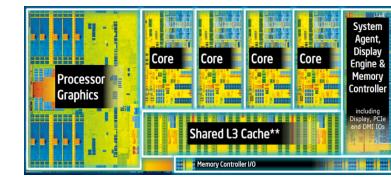
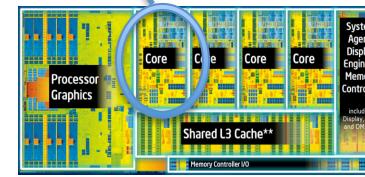
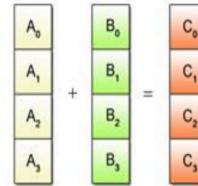
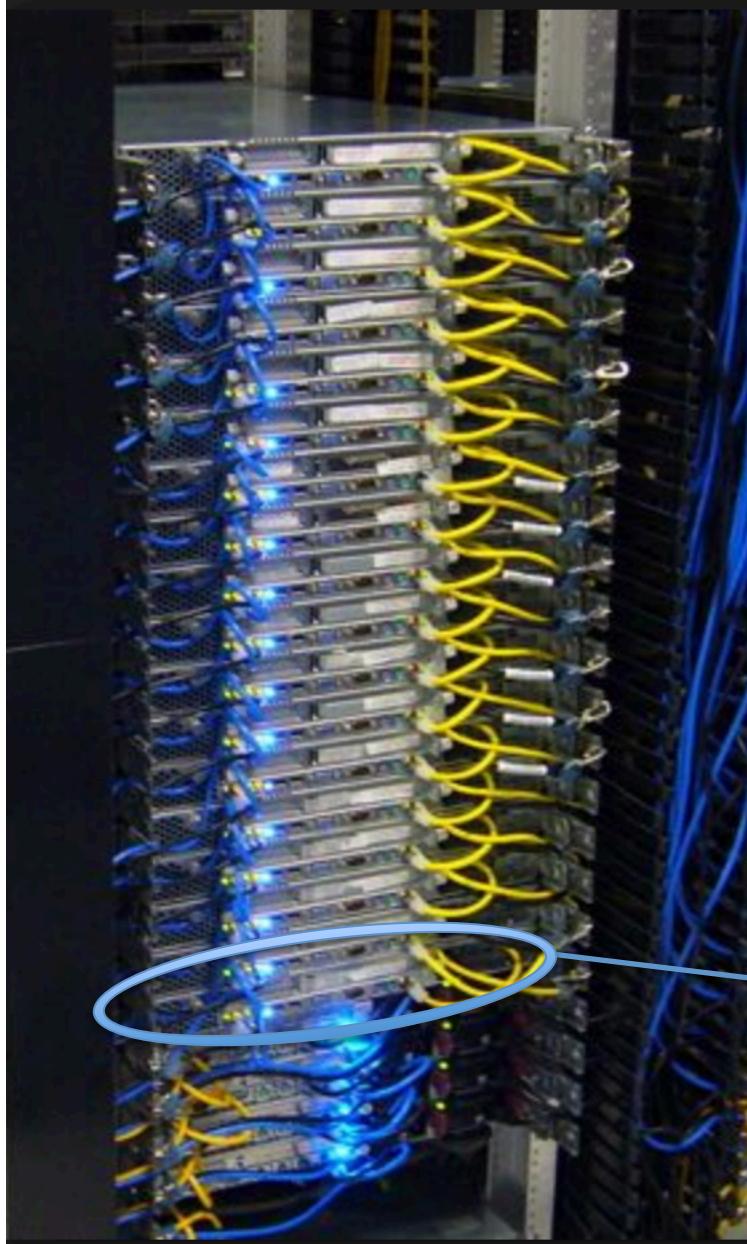


$$\begin{matrix} A_0 \\ A_1 \\ A_2 \\ A_3 \end{matrix} + \begin{matrix} B_0 \\ B_1 \\ B_2 \\ B_3 \end{matrix} = \begin{matrix} C_0 \\ C_1 \\ C_2 \\ C_3 \end{matrix}$$

Server multiprocessore



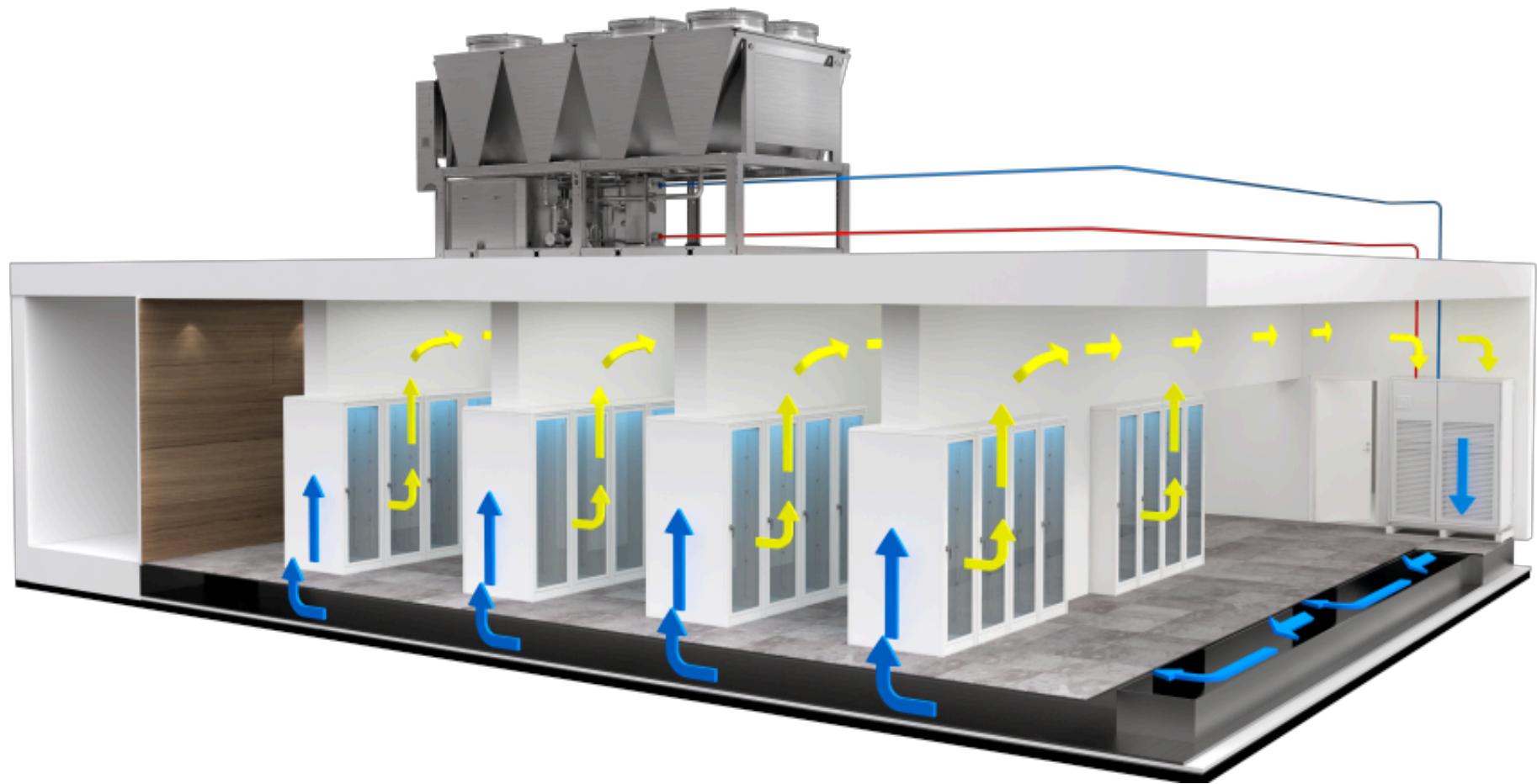
Server rack (cluster)



Data center



Data center



Data center

